

BEHAVIORAL SYNTHESIS AND COMPONENT REUSE WITH VHDL

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Behavioral Synthesis And Component Reuse With Vhdl

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Behavioral Synthesis and Component Reuse with VHDL Ahmed Amine Jerraya, 1997 Improvement in the quality of integrated circuit designs and a designer's productivity can be achieved by a combination of two factors Using more structured design methodologies for extensive reuse of existing components and subsystems It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of methodologies and tools Providing higher level design tools allowing to start from a higher level of abstraction After the success and the widespread acceptance of logic and RTL synthesis the next step is behavioral synthesis commonly called architectural or high level synthesis Behavioral Synthesis and Component Reuse with VHDL provides methods and techniques for VHDL based behavioral synthesis and component reuse The goal is to develop VHDL modeling strategies for emerging behavioral synthesis tools Special attention is given to structured and modular design methods allowing hierarchical behavioral specification and design reuse The goal of this book is not to discuss behavioral synthesis in general or to discuss a specific tool but to describe the specific issues related to behavioral synthesis of VHDL description This book targets designers who have to use behavioral synthesis tools or who wish to discover the real possibilities of this emerging technology The book will also be of interest to teachers and students interested to learn or to teach VHDL based behavioral synthesis

Virtual Components Design and Reuse Ralf Seepold, Natividad Martinez Madrid, 2013-06-29 Design reuse is not just a topic of research but a real industrial necessity in the microelectronic domain and thus driving the competitiveness of relevant areas like for example telecommunication or automotive Most companies have already dedicated a department or a central unit that transfer design reuse into reality All main EDA conferences include a track to the topic and even specific conferences have been established in this area both in the USA and in Europe Virtual Components Design and Reuse presents a selection of articles giving a mature and consolidated perspective to design reuse from different points of view The authors stem from all relevant areas research and academia IP providers EDA vendors and industry Some classical topics in design reuse like specification and generation of components IP retrieval and cataloging or interface customisation are revisited and discussed in depth Moreover new hot topics are presented among them IP quality platform based reuse software IP IP security business models for design reuse and major initiatives like the MEDEA EDA Roadmap

System-on-Chip Methodologies & Design Languages Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field

Design of Hardware/Software Embedded Systems Eugenio Villar Bonet, 2001 Este libro presenta los desafíos planteados por las nuevas y sumamente poderosas tecnologías de integración de sistemas electrónicos que están en la base

de los cambios sociales hacia lo que llaman la Sociedad de la Informaci n en la que los dispositivos electr nicos se har n una parte incorporada de la vida diaria encajados en casi cada producto Es necesario un conocimiento cuidadoso de los desaf os para aprovechar la amplia gama de ocasiones ofrecidas por tales capacidades de integraci n y las correspondientes posibilidades de dise o de sistemas electr nicos

VLSI: Integrated Systems on Silicon Ricardo A. Reis, Luc Claesen, 2013-06-05 This book contains the papers that have been presented at the ninth Very Large Scale Integrated Systems conference VLSI 97 that is organized biannually by IFIP Working Group 10.5 It took place at Hotel Serra Azul in Gramado Brazil from 26-30 August 1997 Previous conferences have taken place in Edinburgh Trondheim Vancouver Munich Grenoble and Tokyo The papers in this book report on all aspects of importance to the design of the current and future integrated systems The current trend towards the realization of versatile Systems on a Chip require attention of embedded hardware software systems dedicated ASIC hardware sensors and actuators mixed analog digital design video and image processing low power battery operation and wireless communication The papers as presented in this book have been organized in two tracks where one is dealing with VLSI System Design and Applications and the other presents VLSI Design Methods and CAD The following topics are addressed VLSI System Design and Applications Track VLSI for Video and Image Processing Microsystem and Mixed mode design Communication And Memory System Design Core voltage Low power Analog Circuits High Speed Circuit Techniques Application Specific DSP Architectures VLSI Design Methods and CAD Track Specification and Simulation at System Level Synthesis and Technology Mapping CAD Techniques for Low Power Design Physical Design Issues in Sub micron Technologies Architectural Design and Synthesis Testing in Complex Mixed Analog and Digital Systems

EDA for IC System Design, Verification, and Testing Louis Scheffer, Luciano Lavagno, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set

System-Level Synthesis Ahmed Amine Jerraya, Jean Mermet, 2012-12-06 System Level Synthesis deals with the concurrent design of electronic applications including both hardware and software The issue has become the bottleneck in the design of electronic systems including both hardware and software in several major industrial fields including telecommunications automotive and aerospace engineering The major difficulty with the subject is that it demands contributions from several research fields including system specification system architecture hardware design and software design Most existing book cover well only a few aspects of system level synthesis The present volume presents a

comprehensive discussion of all the aspects of system level synthesis Each topic is covered by a contribution written by an international authority on the subject **Distributed Embedded Systems: Design, Middleware and Resources** Bernd Kleinjohann, Lisa Kleinjohann, Marilyn Wolf, 2008-07-10 This year the IFIP Working Conference on Distributed and Parallel Embedded Systems DIPES 2008 is held as part of the IFIP World Computer Congress held in Milan on September 7-10 2008 The embedded systems world has a great deal of experience with parallel and distributed computing Many embedded computing systems require the high performance that can be delivered by parallel computing Parallel and distributed computing are often the only ways to deliver adequate real time performance at low power levels This year's conference attracted 30 submissions of which 21 were accepted Prof Jörg Henkel of the University of Karlsruhe graciously contributed a keynote address on embedded computing and reliability We would like to thank all of the program committee members for their diligence Wayne Wolf Bernd Kleinjohann and Lisa Kleinjohann Acknowledgements We would like to thank all people involved in the organization of the IFIP World Computer Congress 2008 especially the IPC Co Chairs Judith Bishop and Ivo De Lotto the Organization Chair Giulio Occhini as well as the Publications Chair John Impagliazzo Further thanks go to the authors for their valuable contributions to DIPES 2008 Last but not least we would like to acknowledge the considerable amount of work and enthusiasm spent by our colleague Claudius Stern in preparing the proceedings of DIPES 2008

Hemad it possible to produce them in their current professional and homogeneous style **2nd Workshop on Libraries, Component Modeling and Quality Assurance** Eugenio Villar Bonet, 1997 Compendio de los trabajos presentados en Toledo durante el 2nd Workshop on Libraries component modeling and quality assurance **SPECC: Specification Language and Methodology** Daniel D. Gajski, Jianwen Zhu, Rainer Dömer, Andreas Gerstlauer, Shuqing Zhao, 2012-12-06 For the near future the recent predictions and roadmaps of silicon semiconductor technology all agree that the number of transistors on a chip will keep growing exponentially according to Moore's Law pushing technology towards the system on a chip SOC era However we are increasingly experiencing a productivity gap where the chip complexity that can be handled by current design teams falls short of the possibilities offered by technological advances Together with growing time to market pressures this drives the need for innovative measures to increase design productivity by orders of magnitude It is commonly agreed that the solutions for achieving such a leap in design productivity lie in a shift of the focus of the design process to higher levels of abstraction on the one hand and in the massive reuse of predesigned complex system components intellectual property IP on the other hand In order to be successful both concepts eventually require the adoption of new languages and methodologies for system design backed up by the availability of a corresponding set of system level design automation tools This book presents the SpecC system level design language SLDL and the corresponding SpecC design methodology The SpecC language is intended for specification and design of SOCs or embedded systems including software and hardware whether using fixed platforms integrating systems from different IPs or synthesizing the system blocks from programming or

hardware description languages SpecC Specification Language and Methodology describes the SpecC methodology that leads designers from an executable specification to an RTL implementation through a well defined sequence of steps Each model is described and guidelines are given for generating these models from executable specifications Finally the SpecC methodology is demonstrated on an industrial size example The design community is now entering the system level of abstraction era and SpecC is the enabling element to achieve a paradigm shift in design culture needed for system product design and manufacturing SpecC Specification Language and Methodology will be of interest to researchers designers and managers dealing with system level design design flows and methodologies as well as students learning system specification modeling and design

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