
Algorithms and Techniques for VLSI Layout Synthesis

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Algorithms and Techniques for VLSI Layout Synthesis Dwight Hill, Don Shugard, John Fishburn, 1988-11-30 Algorithms and Techniques for VLSI Layout Synthesis Dwight Hill, Don Shugard, John Fishburn, Kurt Keutzer, 1988-11-30 **Principles**

of VLSI System Planning Allen M. Dewey, Stephen W. Director, 2012-12-06 This book describes a new type of computer aided VLSI design tool called a VLSI System Planning that is meant to aid designers during the early or conceptual state of design. During this stage of design the objective is to define a general design plan or approach that is likely to result in an efficient implementation satisfying the initial specifications or to determine that the initial specifications are not realizable. A design plan is a collection of high level design decisions. As an example the conceptual design of digital filters involves choosing the type of algorithm to implement e.g. finite impulse response or infinite impulse response the type of polynomial approximation e.g. Equiripple or Chebyshev the fabrication technology e.g. CMOS or BiCMOS and so on. Once a particular design plan is chosen the detailed design phase can begin. It is during this phase that various synthesis simulation layout and test activities occur to refine the conceptual design gradually filling more detail until the design is finally realized. The principal advantage of VLSI System Planning is that the increasingly expensive resources of the detailed design process are more efficiently managed. Costly redesigns are minimized because the detailed design process is guided by a more credible consistent and correct design plan.

The Annealing Algorithm R.H.J.M. Otten, L.P.P.P. van Ginneken, 2012-12-06 The goal of the research out of which this monograph grew was to make annealing as much as possible a general purpose optimization routine. At first glance this may seem a straight forward task for the formulation of its concept suggests applicability to any combinatorial optimization problem. All that is needed to run annealing on such a problem is a unique representation for each configuration a procedure for measuring its quality and a neighbor relation. Much more is needed however for obtaining acceptable results consistently in a reasonably short time. It is even doubtful whether the problem can be formulated such that annealing becomes an adequate approach for all instances of an optimization problem. Questions such as what is the best formulation for a given instance and how should the process be controlled have to be answered. Although much progress has been made in the years after the introduction of the concept into the field of combinatorial optimization in 1981 some important questions still do not have a definitive answer. In this book the reader will find the foundations of annealing in a self contained and consistent presentation. Although the physical analogue from which the concept emanated is mentioned in the first chapter all theory is developed within the framework of Markov chains. To achieve a high degree of instance independence adaptive strategies are introduced.

Testing and Reliable Design of CMOS Circuits Niraj K. Jha, Sandip Kundu, 2012-12-06 In the last few years CMOS technology has become increasingly dominant for realizing Very Large Scale Integrated VLSI circuits. The popularity of this technology is due to its high density and low power requirement. The ability to realize very complex circuits on a single chip has brought about a revolution in the world

of electronics and computers. However, the rapid advancements in this area pose many new problems in the area of testing. Testing has become a very time-consuming process. In order to ease the burden of testing, many schemes for designing the circuit for improved testability have been presented. These design for testability techniques have begun to catch the attention of chip manufacturers. The trend is towards placing increased emphasis on these techniques. Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults. In order to take care of this problem, we need to build fault-tolerant systems. The area of fault-tolerant computing has steadily gained in importance. Today, many universities offer courses in the areas of digital system testing and fault-tolerant computing. Due to the importance of CMOS technology, a significant portion of these courses may be devoted to CMOS testing. This book has been written as a reference text for such courses offered at the senior or graduate level. Familiarity with logic design and switching theory is assumed. The book should also prove to be useful to professionals working in the semiconductor industry.

Hierarchical Modeling for VLSI Circuit Testing Debashis Bhattacharya, John P. Hayes, 2012-12-06 Test generation is one of the most difficult tasks facing the designer of complex VLSI-based digital systems. Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology. It has long been recognized that the testing problem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation; however, the development of such methods has proceeded very slowly. To be acceptable, high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods. The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line (SSL) fault model, which is tightly bound to the gate level of abstraction. This monograph presents a novel approach to solving the foregoing problem. It is based on the systematic use of multibit vectors rather than single bits to represent logic signals, including fault signals. A circuit is viewed as a collection of high level components such as adders, multiplexers, and registers interconnected by n -bit buses. To match this high level circuit model, we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel. However, by reducing the bus size from n to one, we can obtain the traditional gate level circuit and models.

Introduction to Analog VLSI Design Automation Mohammed Ismail, José E. Franca, 2012-12-06 Very large scale integration (VLSI) technologies are now maturing with a current emphasis toward submicron structures and sophisticated applications combining digital as well as analog circuits on a single chip. Abundant examples are found on today's advanced systems for telecommunications, robotics, automotive electronics, image processing, intelligent sensors, etc. Exciting new applications are being unveiled in the field of neural computing, where the massive use of analog/digital VLSI technologies will have a significant impact. To match such a fast technological trend towards single-chip analog/digital VLSI systems, researchers worldwide have long realized the vital need of producing advanced computer-aided tools for designing both

digital and analog circuits and systems for silicon integration Architecture and circuit compilation device sizing and the layout generation are but a few familiar tasks on the world of digital integrated circuit design which can be efficiently accomplished by matured computer aided tools In contrast the art of tools for designing and producing analog or even analog/digital integrated circuits is quite primitive and still lacking the industrial penetration and acceptance already achieved by digital counterparts In fact analog design is commonly perceived to be one of the most knowledge intensive design tasks and analog circuits are still designed largely by hand by expert intimately familiar with nuances of the target application and integrated circuit fabrication process The techniques needed to build good analog circuits seem to exist solely as expertise invested in individual designers

Analog VLSI Implementation of Neural Systems Carver Mead, Mohammed Ismail, 2012-12-06 This volume contains the proceedings of a workshop on Analog Integrated Neural Systems held May 8 1989 in connection with the International Symposium on Circuits and Systems The presentations were chosen to encompass the entire range of topics currently under study in this exciting new discipline Stringent acceptance requirements were placed on contributions 1 each description was required to include detailed characterization of a working chip and 2 each design was not to have been published previously In several cases the status of the project was not known until a few weeks before the meeting date As a result some of the most recent innovative work in the field was presented Because this discipline is evolving rapidly each project is very much a work in progress Authors were asked to devote considerable attention to the shortcomings of their designs as well as to the notable successes they achieved In this way other workers can now avoid stumbling into the same traps and evolution can proceed more rapidly and less painfully The chapters in this volume are presented in the same order as the corresponding presentations at the workshop The first two chapters are concerned with finding solutions to complex optimization problems under a predefined set of constraints The first chapter reports what is to the best of our knowledge the first neural chip design In each case the physics of the underlying electronic medium is used to represent a cost function in a natural way using only nearest neighbor connectivity

Steady-State Methods for Simulating Analog and Microwave Circuits Kenneth S. Kundert, Jacob K. White, Alberto L. Sangiovanni-Vincentelli, 2013-03-09 The motivation for starting the work described in this book was the interest that Hewlett Packard's microwave circuit designers had in simulation techniques that could tackle the problem of finding steady state solutions for nonlinear circuits particularly circuits containing distributed elements such as transmission lines Examining the problem of computing steady state solutions in this context has led to a collection of novel numerical algorithms which we have gathered along with some background material into this book Although we wished to appeal to as broad an audience as possible to treat the subject in depth required maintaining a narrow focus Our compromise was to assume that the reader is familiar with basic numerical methods such as might be found in Dahlquist⁷⁴ or Vlach⁸³ but not assume any specialized knowledge of methods for steady state problems Although we focus on algorithms for computing steady state solutions of

analog and microwave circuits the methods herein are general in nature and may find use in other disciplines A number of new algorithms are presented the contributions primarily centering around new approaches to harmonic balance and mixed frequency time methods These methods are described along with appropriate background material in what we hope is a reasonably satisfying blend of theory practice and results The theory is given so that the algorithms can be fully understood and their correctness established

VLSI Design for Manufacturing: Yield Enhancement Stephen W.

Director, Wojciech Maly, Andrzej J. Strojwas, 2012-12-06 One of the keys to success in the IC industry is getting a new product to market in a timely fashion and being able to produce that product with sufficient yield to be profitable There are two ways to increase yield by improving the control of the manufacturing process and by designing the process and the circuits in such a way as to minimize the effect of the inherent variations of the process on performance The latter is typically referred to as design for manufacture or statistical design As device sizes continue to shrink the effects of the inherent fluctuations in the IC fabrication process will have an even more obvious effect on circuit performance And design for manufacture will increase in importance We have been working in the area of statistically based computer aided design for more than 13 years During the last decade we have been working with each other and individually with our students to develop methods and CAD tools that can be used to improve yield during the design and manufacturing phases of IC realization This effort has resulted in a large number of publications that have appeared in a variety of journals and conference proceedings Thus our motivation in writing this book is to put in one place a description of our approach to IC yield enhancement While the work that is contained in this book has appeared in the open literature we have attempted to use a consistent notation throughout this book

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