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IEEE ACM International Conference on Computer-Aided Design ICCAD-96, a Conference for the EE CAD Professional, November 10-14, 1996, Red Lion Hotel, San Jose, California IEEE/ACM International Conference on Computer-Aided Design (1996 : San Jose),IEEE Circuits and Systems Society,IEEE Computer Society,ACM Special Interest Group on Design Automation,1996 *1996 IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 1996 San Jose, California* ,1996 **Digest of Technical Papers** ,1999 **Boolean Circuit Rewiring** Tak-Kei Lam,Wai-Chung Tang,Xing Wei,Yi Diao,David Yu-Liang Wu,2016-01-06 Demonstrates techniques which will allow rewiring rates of over 95% enabling adoption of deep sub micron chips for industrial applications Logic synthesis is an essential part of the modern digital IC design process in semiconductor industry This book discusses a logic synthesis technique called rewiring and its latest technical advancement in terms of rewirability Rewiring technique has surfaced in academic research since 1993 and there is currently no book available on the market which systematically and comprehensively discusses this rewiring technology The authors cover logic transformation techniques with concentration on rewiring For many decades the effect of wiring on logic structures has been ignored due to an ideal view of wires and their negligible role in the circuit performance However in today's semiconductor technology wiring is the major player in circuit performance degeneration and logic synthesis engines can be improved to deal with this through wire based transformations This book introduces the automatic test pattern generation ATPG based rewiring techniques which are recently active in the realm of logic synthesis verification of VLSI SOC designs Unique comprehensive coverage of semiconductor rewiring techniques written by leading researchers in the field Provides complete coverage of rewiring from an introductory to intermediate level Rewiring is explained as a flexible technique for Boolean logic synthesis introducing the concept of Boolean circuit transformation and testing with examples Readers can directly apply the described techniques to real world VLSI design issues Focuses on the automatic test pattern generation ATPG based rewiring methods although some non ATPG based rewiring methods such as graph based alternative wiring GBAW and set of pairs of functions to be distinguished SPFD based rewiring are also discussed A valuable resource for researchers and postgraduate students in VLSI and SoC design as well as digital design engineers EDA software developers and design automation experts that specialize in the synthesis and optimization of logical circuits

Proceedings of the 1999 International Conference on Software Engineering ,1999 Extreme Statistics in Nanoscale Memory Design Amith Singhee,Rob A. Rutenbar,2010-09-09 Knowledge exists you only have to find it VLSI design has come to an important inflection point with the appearance of large manufacturing variations as semiconductor technology has moved to 45 nm feature sizes and below If we ignore the random variations in the manufacturing process simulation based design essentially becomes useless since its predictions will be far from the reality of manufactured ICs On the other hand using design margins based on some traditional notion of worst case scenarios can force us to sacrifice too much in terms of power

consumption or manufacturing cost to the extent of making the design goals even infeasible. We absolutely need to explicitly account for the statistics of this random variability to have design margins that are accurate so that we can find the optimum balance between yield loss and design cost. This discontinuity in design processes has led many researchers to develop effective methods of statistical design where the designer can simulate not just the behavior of the nominal design but the expected statistics of the behavior in manufactured ICs. Memory circuits tend to be the hardest hit by the problem of these random variations because of their high replication count on any single chip which demands a very high statistical quality from the product.

Requirements of 5.6s.0

Computer-Aided Design of Analog Integrated Circuits and Systems Rob A. Rutenbar, Georges G. E. Gielen, 2002-05-06

The tools and techniques you need to break the analog design bottleneck. Ten years ago analog seemed to be a dead end technology. Today System on Chip SoC designs are increasingly mixed signal designs. With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process. Today designers are moving beyond hand crafted one transistor at a time methods. They are using new circuit and physical synthesis tools to design practical analog circuits, new modeling and analysis tools to allow rapid exploration of system level alternatives, and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago. To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field, this volume collects in one place the essential set of analog CAD papers that form the foundation of today's new analog design automation tools. Areas covered are Analog synthesis, Symbolic analysis, Analog layout, Analog modeling and analysis, Specialized analog simulation, Circuit centering and yield optimization, Circuit testing.

Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck.

The Best of ICCAD Andreas Kuehlmann, 2012-12-06

In 2002 the International Conference on Computer Aided Design ICCAD celebrates its 20th anniversary. This book commemorates contributions made by ICCAD to the broad field of design automation during that time. The foundation of ICCAD in 1982 coincided with the growth of Large Scale Integration. The sharply increased functionality of board level circuits led to a major demand for more powerful Electronic Design Automation EDA tools. At the same time LSI grew quickly and advanced circuit integration became widely available. This in turn required new tools using sophisticated modeling, analysis, and optimization algorithms in order to manage the evermore complex design processes. Not surprisingly during the same period a number of start up companies began to commercialize EDA solutions complementing various existing in house efforts. The overall increased interest in Design Automation DA required a new forum for the emerging community of EDA professionals, one which would be focused on the publication of high quality research results and provide a structure for the exchange of ideas on a broad scale. Many of the original ICCAD

volunteers were also members of CANDE Computer Aided Network Design a workshop of the IEEE Circuits and System Society In fact it was at a CANDE workshop that Bill McCalla suggested the creation of a conference for the EDA professional Bill later developed the name **High Data Rate Transmitter Circuits** C.J. de Ranter, Michiel Steyaert, 2006-04-18 High Data Rate Transmitter Circuits is a practical guide and introduction to the design of key RF building blocks used in high data rate transmitters The emphasis lies on CMOS circuit techniques applicable to oscillators and upconvertors Furthermore a method for RF specific design automation is exemplified by the CYCLONE tool for automated LC VCO synthesis Written in an easily accessible manner High Data Rate Transmitter Circuits is essential reading for both students and practicing engineers interested in analog RF design and RF specific design automation The book has been praised for its pleasant and light style of writing without losing detail on the technical side

Electronic System-Level HW/SW Co-Design of Heterogeneous Multi-Processor Embedded Systems Luigi Pomante, 2016-06-15 Modern electronic systems consist of a fairly heterogeneous set of components Today a single system can be constituted by a hardware platform frequently composed of a mix of analog and digital components and by several software application layers The hardware can include several heterogeneous microprocessors e.g. GPP, DSP, GPU etc. dedicated ICs, ASICs and/or FPGAs, memories, a set of local connections between the system components and some interfaces between the system and the environment, sensors, actuators etc. Therefore on the one hand multi-processor embedded systems are capable of meeting the demand of processing power and flexibility of complex applications On the other hand such systems are very complex to design and optimize so that the design methodology plays a major role in determining the success of the products For these reasons to cope with the increasing system complexity the approaches typically used today are oriented towards co-design methodologies working at the higher levels of abstraction Unfortunately such methodologies are typically customized for the specific application, suffer of a lack of generality and still need a considerable effort when real size projects are envisioned Therefore there is still the need for a general methodology able to support the designer during the high level steps of a co-design flow, enabling an effective design space exploration before tackling the low level steps and thus committing to the final technology This should prevent costly redesign loops In such a context the work described in this book, composed of two parts, aims at providing models, methodologies and tools to support each step of the co-design flow of embedded systems implemented by exploiting heterogeneous multi-processor architectures mapped on distributed systems as well as fully integrated onto a single chip The first part focuses on issues like the analysis of system specification languages and the analysis of existing system level HW/SW co-simulation methodologies to support heterogeneous multi-processor architectures The second part focuses mainly on Design Space Exploration and it presents both some theoretical advancements with respect to the first part and the development of a prototypical framework that provides practical exploitation of the proposed concepts

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